Code: 9A04706 **R09**

B.Tech IV Year I Semester (R09) Regular & Supplementary Examinations December 2015

DIGITAL DESIGN THROUGH VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain about Test bench.
(b) List out Verilog key-words and operators.
(c) Define functional verification of Verilog HDL.

2 (a) Draw the logic symbols of Tristate gates and explain them.
(b) Realize T-FF using JK-FF and SR-FF.

3 (a) Write the Verilog code for 2 x 4 decoder using behavioral model.
(b) Write the Verilog code 1 x 8 demultiplexer using behavioral model.

4 (a) Design Half adder using switch level modeling.
(b) Design Full adder using data flow model.

5 (a) Write the difference between Moore and Mealy with examples.
(b) Write Verilog HDL for CMOS NAND gate using switch level modeling.

6 (a) What is SM chart? Explain the basic blocks with examples.
(b) Explain about linked state machines.

7 (a) Explain about ALTERA FLEX 10K series CPLD.
(b) Differentiate FPGAs and CPLDs.

8 (a) Explain about UART design Verilog model.
(b) Explain about static RAM memory Verilog model.

*****