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R07

B.Tech II Year I Semester (R07) Supplementary Examinations December 2015 PULSE & DIGITAL CIRCUITS

(Common to EEE & EIE) (For 2008 Regular admitted batch only)

Time: 3 hours

Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

- 1 (a) Explain the step response of compensated attenuator.
 - (b) Assuming the capacitor to be initially unchanged, determine the output response of the low pass Rc circuit with time constant 0.05 ms to the input waveform shown in figure below.



- 2 (a) Draw and explain the transfer characteristics of emitter coupled clipper.
 - (b) Explain the effect of Rs and Rf on clamper circuit.
- 3 (a) Explain how transistor can be used as a switch in the circuit, under what conditions a transistor is said to be OFF and ON, respectively.
 - (b) Derive the expression for collector to emitter voltage with open circuited base.
- 4 (a) Determine the value of capacitors to be used in an astable multivibrator to provide a train of pulse 2 μs wide at a repetition rate of 100 kHz. If $R_1 = R_2 = 20 k\Omega$.
 - (b) Explain about various switching conditions of Schmitt trigger.
- 5 (a) With circuit diagram and relevant waveforms explain the operation of a transistor bootstrap time base generator.
 - (b) Derive the expression for mathematical relationship between sweep speed error, displacement error and transmission error for an exponential sweep circuit.
- 6 (a) With the help of neat waveform explain the synchronization with frequency division.
 - (b) Explain synchronization using monostable symmetrical signals.
- 7 (a) What is sampling gate? Explain how it differs from logic gates.
 - (b) List the advantages of bidirectional sampling gate using two transistors.
- 8 (a) Draw and explain the circuit of AND gate using diodes.
 - (b) Draw the circuit diagrams and explain the working of a diode transistor logic.

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