Code: R7210204

R07

B.Tech II Year I Semester (R07) Supplementary Examinations December 2015

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E & ECC)

(For 2008 regular admitted batch only)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) If $32_{10} = x_2 = y_8$, than determine x and y.

(b) Explain about 1's complement and 2's complement of a number.

2 (a) Prove that $a + a'b = a + b$.

(b) Convert the following SOP into POS:
$F = ABC + BCD + AC'$.

(c) Implement the following using universal gates:
(i) $(A' + C)(AC' + BC)$.
(ii) $AB' + (B' + C')A'$.

3 (a) Simplify the following using Karnaugh map:
$F = \Sigma\, m(1, 2, 3, 4, 5, 7, 9)$.

(b) What is a tabulation method? State its advantages compared to Karnaugh map by taking an example.

4 (a) Design a Grey code to binary converter and realize it.

(b) Draw and explain the logic diagram of a 2 line to 4 line decoder – DE multiplexer using NOR gates only.

5 (a) Implement the following using PLA $f(a, b, c, d) = \Sigma\, m(0, 2, 6, 7, 8, 9, 12, 13, 14)$.

(b) What are different PLD's? Explain them.

6 (a) Convert JK flip-flop into SR flip-flop.

(b) Explain about master slave flip-flop.

(c) Explain about the Johnson counter.

7 (a) Explain about finite state machines and enumerate their capabilities and limitations.

(b) Enumerate the steps in the conversion of Mealy machine into Moore machine.

8 (a) Explain the multiplexer method of implementing ASM charts.

(b) Explain the control subsystem implementation of weighting machine.

*****