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Code: 9A04306 **R09**

B.Tech II Year I Semester (R09) Supplementary Examinations December 2015

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

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1 (a) Compute the addition and convert the result into hexadecimal $(1234)_8 + (1111)_8 + (3456)_8$.
(b) Convert the following into decimal numbers:
(i) $(ABD)_{16}$. (ii) $(98)_{16}$.

2 (a) Represent the following Boolean expressions with minimum number of gates:
(i) $(AB + AB^{I})\ (AB^{I})$.
(ii) $[(ABC\ (C + D + E)) + (A + DBC)^{I}]\ (ABC + (CAD)^{I})$.
(b) Realize basic gates with universal gates.

3 Simplify the following expression using K-map method.
$Y(A, B, C, D) = \sum m\ (0, 2, 5, 7, 8, 10, 13, 15)$.

4 (a) Draw and explain the operation of a 4-bit serial adder.
(b) Give the comparison between serial adder and parallel adder.

5 (a) Draw the logic diagram of JK master slave flip-flop.
(b) Explain HDL for sequential circuit giving example.

6 (a) Draw and explain the mod-10 counter.
(b) Explain the operation of universal shift register with the help of diagram.

7 (a) Discuss various read only memory.
(b) List the applications of PLA.

8 (a) What is a latch? How it is different from flip-flop?
(b) Design any one asynchronous sequential logic circuit.

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