Code: 13A04306 **R13**

B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015

DIGITAL LOGIC DESIGN

(Common to IT and CSE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Determine the value of base 'X' if $(225)_x = (341)_8$.
(b) Find the complement of the function, F = x (y'z' + yz) by taking their duals and complementing each literal.
(c) Define don't care condition with an example.
(d) Implement EX-OR gate using only NAND gates.
(e) Define priority encoder.
(f) Give the design procedure for the design of a combinational circuit.
(g) What is race around condition? How can we eliminate the race around condition?
(h) Define shift registers.
(i) What are the differences between PLA and PAL?
(j) Define fan out of a logic gate.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Convert the following $(3456)_8$ to base 3 and base 7.
(b) Using 2's complement, perform $(42)_{10}$-$(68)_{10}$

OR

3 (a) Simplify the following three variable expression using Boolean algebra: Y = ∑m(1, 3, 5, 7).
(b) Convert the given expression in standard POS form: Y = A.(A + B + C)

UNIT - II

4 (a) Minimize the following function using Karnaugh map method.
f(w,x,y,z)= ∑m(0,7,8,9,10,12) + ∑d (2,5,13)
(b) Implement the following function in NAND-NAND two level forms and draw the circuits.
Y = AC+ABC+A'BC+AB+D

OR

5 Minimize the following function using tabular method.
f(A,B,C,D) = ∑m(0,1,9,15,24,29,30) + ∑d (8,11,31)

UNIT - III

6 (a) Design and draw a full adder circuit.
(b) Implement the following Boolean function using 4 x 1 MUX.
F(a,b,c) = ∑m (1,3,5,6)

OR

7 Design 2 bit magnitude comparator and draw its logic circuit diagram.

UNIT - IV

8 (a) Draw and explain the operation of RS flip-flop.
(b) Design and draw the 3 bit up-down synchronous counter.

OR

9 What are the different types of shift registers? Explain any one type of shift register.

UNIT - V

10 Implement the following functions using PLA.
A (x,y,z)= ∑m (1,2,4,6)
B (x,y,z) = ∑m (0,1,6,7)
C (x,y,z) = ∑m (2,6)

OR

11 (a) Differentiate between RAM and ROM.
(b) Draw and explain the operation of 2 input TTL NAND gate with totem pole output.

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