

Code: R7220404

B.Tech II Year II Semester (R07) Supplementary Examinations December/January 2015/2016

SWITCHING THEORY & LOGIC DESIGN
(Electronics & Communication Engineering)

(For 2008 Regular admitted batch only)

Time: 3 hours

Max. Marks: 80

Answer any FIVE questions
All questions carry equal marks

- 1 (a) Explain about error correcting codes.
(b) $A = 1010.1$, $B = 101.01$; find A/B .
- 2 (a) Describe basic Boolean algebra theorems and its properties.
(b) Show that the dual of the exclusive OR is equal to its complement.
- 3 (a) Convert into canonical POS form: $f = \sum m(2,3,5,7,10,11,14)$.
(b) Minimize the following function using tabular minimization.
$$F(A, B, C, D) = \sum m(1,2,3,5,9,12,14,15) + d(4,8,11).$$
- 4 (a) Write design procedure of combinational logic circuits.
(b) Realize the Boolean function $T(X, Y, Z) = \sum(1,3,4,5)$ using logic gates for hazard free.
- 5 (a) Discuss the functionality of PLA. How its programming table is prepared?
(b) Explain about the structure of PROM with a help of schematic diagram.
- 6 (a) Convert SR flip flop to T flip flop.
(b) Write a detailed note on PLDs.
- 7 (a) Explain the limitations and capabilities of finite state machine.
(b) Discuss about minimization of completely specified and incompletely specified sequential machines.
- 8 (a) Obtain the ASM chart for the following state transition.
Start for state T1; then if $xy = 00$, go to T2 if $xy = 01$, go to T3; if $xy = 10$ go to T1; otherwise go to T3.
(b) How do you indicate Moore and Mealy output in an ASM chart? Show an example.
