

Code: 9A02405

**R09** 

B.Tech II Year II Semester (R09) Supplementary Examinations December/January 2015/2016

## **ANALOG ELECTRONIC CIRCUITS**

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions All questions carry equal marks

- (a) Compare the small signal model of BJT and FET.
  - (b) For a CB transistor amplifier driven by a voltage source of internal resistance  $R_s = 600 \,\Omega$ , the load impedance is a resistor  $R_L = 1200 \,\Omega$ . The h-parameters are  $h_{ib} = 22 \,\Omega$ ,  $h_{rb} = 4 \,\mathrm{X} \,10^{-4}$ ,  $h_{fb} = -0.98$  and  $h_{ob} = 0.25 \,\mu\text{A/V}$ . Compute the current gain  $A_{I}$ , the input impedance  $R_{i}$ , voltage gain  $A_{v}$ , overall voltage gain  $A_{vs}$  overall current gain  $A_{IS}$ , output impedance  $Z_{o}$  and power gain  $A_{p}$ .
- Draw the hybrid  $\pi$  model of a transistor and derive its parameters and explain its frequency response.
- 3 (a) Explain with diagrams of Feedback topologies.
  - (b) An amplifier has an open loop gain of 90. When a negative feedback of feedback factor 0.6 is applied to it, calculate the overall gain.
- 4 (a) Draw the circuit of FET RC phase shift oscillator and derive its frequency oscillations using its equivalent circuit.
  - (b) Design a Colpitts oscillator with voltage gain of 50 and frequency of oscillation is 25 kHz.
- 5 (a) Define about class A, class B, class AB and class C operation of power amplifiers.
  - (b) Design a class B power amplifiers to deliver 25 W to a load resistor  $R_L = 8 \Omega$ , using transformer coupling.  $V_m = V_{CC} = 25 \text{ V}$ . Assume reasonable data wherever necessary.
- 6 (a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.
  - (b) Explain the effect of diode characteristics on clamping voltage.
- 7 Write short notes on:
  - (a) BJT as a switch.
  - (b) Latching phenomena in a transistor.
- 8 (a) Discuss the different methods of triggering a flip-flop. Explain the role of commutating capacitors in a binary circuit.
  - (b) Draw the circuit diagram of a fixed bias binary with speed up capacitors.

\*\*\*\*