Code: 9A04401 **R09**

B.Tech II Year II Semester (R09) Supplementary Examinations December/January 2015/2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain Gray code with its advantages.
(b) List the XS3 code for decimal 0 to 9.
(c) What are the rules for XS3 addition? Add the two decimal numbers 23 and 58 in XS3 code.

2 (a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
(b) Prove the identity of the following Boolean equations:
(i) x'y' + x'y + xy = x' + y.
(ii) a'b + b'c' + ab + b'c =1.
(c) Implement the Boolean function F = A (B + CD) + BC' using only NAND gates.

3 (a) What are the advantages of tabulation method over K-map?
(b) Simplify the following Boolean function using Tabulation method:
Y(A,B,C,D) = ∑(0,1,2,3,5,7,8,9,11,14)

4 (a) Design BCD to XS3 code converter using a 4 bit Full-adders MSI circuit.
(b) What is Hazard in switching circuits? Explain the design of Hazard free switching circuit with an example.

5 (a) Design a combinational circuit using ROM that accepts 3-bit number and generates output binary number equal to the square of the input number.
(b) Write short notes on types of read only memory.

6 (a) Design Mod-10 synchronous counter using J-K flip-flop
(b) Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S1	S0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

7 (a) Distinguish between mealy and moore machines?
(b) Find the equivalence partition for the given machine and standard form of corresponding reduced machine.

PS	NS, Z	
	X=0	X=1
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	C, 1	E, 0
E	B, 0	D, 0

8 Design a half adder and half subtractor circuit using multiplexer.

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