Code: 9A04404 **R09**

B.Tech II Year II Semester (R09) Supplementary Examinations December/January 2015/2016

PULSE & DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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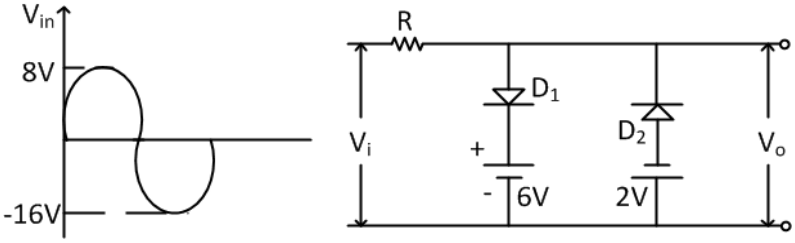
1 (a) Obtain the response of high pass RC circuit for a ramp input wave form.
(b) Write short notes on RLC circuit.

2 (a) State and prove clamping circuit Theorem.
(b) Determine V_0 for the network shown in figure for the given wave form? Assume ideal diodes.



3 (a) Explain the phenomenon of "Latching" in a transistor switch.
(b) Explain with relevant diagram the various transistor switching times.

4 (a) Explain different triggering methods of binary circuits.
(b) A collector coupled Fixed bias binary uses NPN transistors with h_{FE} = 100. The circuit parameters are V_{CC} = 12 V, V_{BB} = - 3 V, R_C = 1 kΩ, R_1 = 5 kΩ, and R_2 = 10 kΩ. Verify that when one transistor is cut-off the other is in saturation. Find the stable state currents and voltages for the circuit. Assume for transistors $V_{CE}(sat)$ = 0.3 V and $V_{BE}(sat)$ = 0.7 V.

5 (a) Compare miller and boot strap circuits.
(b) Derive the expression for slope error of bootstrap circuit.
(c) Explain about double bootstrapping.

6 (a) What are different factors that cause phase delay?
(b) What is 6 to 1 frequency division? Explain.

7 (a) Compare sine wave synchronization with pulse synchronization.
(b) With the help of neat waveforms explain Sine Wave frequency division with a sweep circuit.

8 (a) Design OR and NAND by using CMOS.
(b) What are the advantages and disadvantages of open collector outputs?

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