Code: R7310404

R07

B.Tech III Year I Semester (R07) Supplementary Examinations December 2015

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

(For 2008 regular admitted batch only)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the effect of floating inputs on CMOS gate.
(b) Explain how a CMOS device is destroyed.
(c) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic.

2 (a) Draw the circuit diagram of basic CMS gate and explain the operation.
(b) Discuss the steps in VHDL design flow.

3 (a) Design the logic circuit and write a data-flow style VHDL program for the following function:
$F(A) = \Pi_{P, Q, R, S}(1, 3, 4, 5, 6, 7, 9, 12, 13, 14)$
(b) Design a logic circuit to detect prime number of a 5-bit input.

4 (a) With the help of logic diagram explain 74 X 157 multiplexer.
(b) Write the data flow style VHDL program for this IC.

5 What is 74 X 138? Give the logic symbol for 74 X 138 and write a VHDL code in structural model.

6 What is a comparator? Explain the operation of a 2-bit comparator with a relevant diagram. Draw its logic symbol and write a VHDL code for it.

7 (a) Distinguish between the synchronous and asynchronous counters.
(b) Design a 4 bit binary synchronous counter using 74 X 74. Write a VHDL code for it using data flow style.

8 Draw and explain the structure of an 8 X 4 static RAM.

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