Code: 9A04401 **R09**

B.Tech III Year I Semester (R09) Supplementary Examinations December 2015

SWITCHING THEORY & LOGIC DESIGN

(Mechatronics)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Give the various ways of representing negative numbers in binary system.
(b) Construct a seven bit error correcting code to represent the decimal digits by augmenting the Excess – 3 code and use odd – 1 check.

2 (a) What Boolean theorems are used for the following in simplifying switching functions:
(i) Combining terms. (ii) Eliminating terms. (iii) Eliminating literals. (iv) Factoring.
(b) Realize the following expression using optimum NAND gates:
$f = a'bc + ab'c + abc + abc'$

3 (a) Define minterm and maxterm.
(b) List the product term implicants of $f = F(abc) = \sum m(0,1,5,70)$ and separate prime implicants. Why is "a′c" is not a prime implicant?

4 (a) Design 8 – 4 – 2 – 1 code converter to drive an seven segment indicator.
(b) Realize the following function using multiplexer:
$f = a'bc + ac' + b'cd'$

5 Explain the realization of switching function using ROM, implement the following functions using ROM: $f = a'bc + ac' + b'cd'$; $f = a'bc + ab'c + abc + abc'$

6 Explain various steps in a synchronous sequential circuit design by taking the example, design of a sequence detector with input X and one output Z, the output is Z = 1, if the total number of 1's received is divisible by 3.

7 Explain the design of a binary multiplier with its data path and control unit. Draw the ASM chart of the above control unit.

8 Reduce the following state table to a minimum number of rows (states) using implication chart, make a suitable state assignment and realize the FSM using D-flip-flop.

Present state	Next state		Output
	X = 0	X = 1	
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	G	E	0

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