Code: 9A15502 **R09**

B.Tech III Year I Semester (R09) Supplementary Examinations December 2015

DIGITAL SYSTEM DESIGN

(Computer Science & Systems Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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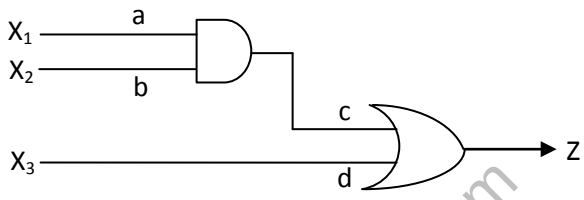
1 (a) What are the basic building blocks of an ASM chart? Explain about them.
(b) Discuss in detail about reduction of state tables and state assignments.

2 (a) Describe the PLA minimization technique with examples.
(b) Write short notes on the test generation for the faults in PLA.

3 (a) Explain folding theorem. What are the necessary and required conditions to fold a PLA along the column to have maximum folding?
(b) For the circuit shown in figure below, find a minimum test set for all the stuck at faults by the fault table method.



4 (a) Describe the algorithmic steps involved in PODEM.
(b) What do you mean by a fault in a circuit? How do you classify the faults in a circuit explain them?

5 (a) Discuss about the following types of faults:
(i) Stuck at faults. (ii) Bridge faults. (iii) Temporary faults.
(b) A two level AND – OR network realizes the function $f = 0200 + 1002 + 2121$. Find the minimum test set to detect all the faults using Kohavi algorithm.

6 (a) Discuss about the following terms:
(i) Flow table. (ii) Cycles and hazards.
(b) With respect to an asynchronous sequential machine, explain about minimal closed corners.

7 (a) What is a diagnosable sequential machine? Discuss the design of definitely diagnosable machine.
(b) Prove that every n-state machine has an adaptive homing sequence whose length is at most (n-1)n /2.

8 (a) Contrast the structures of FPGA's and CPLD's.
(b) Construct the fault detection experiment for the machine shown below.

PS	N S, Z	
	X = 0	X = 1
A	B, 0	C, 1
B	C, 0	D, 0
C	D, 1	C, 1
D	A, 1	B, 0