Code: 13A04504 **R13**

B.Tech III Year I Semester (R13) Regular Examinations December 2015

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics

(b) What is noise margin? Find out the noise margin from the actual characteristics of the inverter

(c) Draw the transition times for CMOS circuits with: (i) ideal case of zero-time switching. (ii) a more realistic approximation. (iii) Actual timing, showing rise and fall times.

(d) What are the various steps in an HDL-based design flow?

(e) What is a register? How many different types data can be entered and retrieved?

(f) What is mean by Universal Register? Name any one commercial universal register.

(g) Distinguish between Mealy and Moore machines with suitable diagrams.

(h) A sequence detector produces a '1' for each occurrence of the input sequence '1001' at its input. Draw the state-transition diagram of the FSM realizing the sequence detector.

(i) What is meant by PLD? What are the advantages of PLDs?

(j) Explain positive and negative edge triggered Flip-Flops.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.

(b) Draw neat circuit diagram, function table and logic symbol of a 2- input CMOS NAND gate.

OR

3 (a) Explain the principle of a Emitter-Coupled Logic (ECL/CML) through Basic ECL inverter/buffer circuit with input HIGH and LOW.

(b) What are the advantages and disadvantages of ECL?

UNIT – II

4 (a) Draw the VHDL program file structure and explain the same with the syntax of a VHDL entity declaration and architecture definition.

(b) Write the syntax of a VHDL function definition and write a VHDL function for converting STD_LOGIC_VECTOR to INTEGER.

OR

5 (a) Write the syntax of a VHDL component declaration and by making use of component declaration write a VHDL program for a prime-number detector.

(b) Write the syntax of a VHDL process statement and by making use of process statements write a process-based dataflow VHDL architecture for the prime-number detector.

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UNIT – III

6 Draw the logic symbol, truth table, logic diagram of a commercially available MSI 74x138 3-to-8 binary decoder and model the same using data flow-style VHDL program.

OR

7 Draw the logic symbol, truth table, logic diagram of a commercially available MSI 74x157 2-input, 4-bit multiplexer and model the same using behavioral-style VHDL program.

UNIT – IV

8 Draw the logic symbol, arithmetic conditions, logic diagram of a commercially available MSI 74x682 8-bit comparator and model the same using VHDL program.

OR

9 Describe the internal structure, functional operation and timing of edge-triggered commercially available SSI 74x74 D flip-flop and model the same using behavioral-style VHDL program with preset and clear.

UNIT – V

10 (a) Draw the logic diagram of a simple 8x4 diode ROM and explain its operation.
(b) List out commercial ROM types and compare them with respect to technology, read cycle, write cycle and comment on each one.
(c) How the limitations of a ROM-based realization are overcome in a PLA based realization?

OR

11 (a) Sketch the basic structure of a 2^n x b RAM and functional behavior of a SRAM cell.
(b) Explain how read and write operations are performed in a SRAM with the help of timing diagrams.
(c) In what way the DRAMs differ from SRAMs? Explain the read and write operations for one transistor DRAM cell.

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