Code: 13A04509 **R13**

B.Tech III Year I Semester (R13) Regular Examinations December 2015

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Give the classification of ICs.
(b) What is the significance of an AC amplifier?
(c) Define comparator.
(d) Draw the block schematic of the PLL.
(e) Draw the basic CMOS inverter circuit.
(f) List the characteristics of Emitter Coupled Logic (ECL).
(g) List the features of VHDL.
(h) What are the different ways to specify a time delay in a VHDL code?
(i) Give the importance of three state devices.
(j) Define clock skew.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Define the following:
(i) CMRR. (ii) PSRR. (iii) Slew rate.
(b) Draw and explain the operation of current to voltage converter

OR

3 (a) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 kHz.
(b) Discuss the different types of linear IC packages.

UNIT – II

4 (a) Explain any two applications of PLL.
(b) Draw and explain the operation of Antilog amplifier.

OR

5 (a) A Schmitt trigger with the upper threshold level V_{UT} = 0 V and hysteresis width V_H = 0.2 V converts a 1 kHz sine wave of amplitude $4V_{PP}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.
(b) With a neat sketch explain the operation of triangular waveform generator.

UNIT – III

6 (a) Give the comparison of logic families.
(b) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.

OR

7 (a) Discuss in brief about CMOS/TTL interfacing.
(b) Explain the following terms with reference to CMOS logic:
(i) Logic levels. (ii) Power supply rails

UNIT – IV

8 Explain in detail about the steps involved in HDL-based design flow.

OR

9 (a) Explain with an example, the syntax and the function of the following VHDL statements:
(i) Case statement. (ii) Loop statement.
(b) Write a brief note on simulation.

UNIT – V

10 Design a logic circuit of Binary to Gray code converter and write a data flow VHDL program.

OR

11 (a) Design a conversion circuit to convert a T flip-flop from D flip-flop.
(b) Give the comparison between Moore and Mealy circuits.

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