**Code: R7320206**

**R07**

B.Tech III Year II Semester (R07) Supplementary Examinations December/January 2015/2016

**VLSI DESIGN**

(Common to EEE, E.Con.E and ECE)

(For 2008 regular admitted batch only)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) What are the advantages of CMOS technology?

(b) Draw the flow chart for VLSI design flow and explain clearly about each step.

2 Draw the small signal AC characteristics of MOS transistor. And derive expression for $g_m$ in different regions.

3 Draw CMOS inverter, its physical lay out with its stick diagram.

4 (a) What is a transmission gate? Explain clearly about it. Draw the symbols of transmission gate.

(b) Implement XOR gate using transmission gate.

5 (a) Write about switch logic.

(b) Implement 4:1 multiplexer using Switch logic and compare it with gate logic implementation?

6 (a) Discriminate between testing and simulation in IC designing.

(b) Implement the following function using PAL:

$f_1 = \overline{ABC} + AB + BC + CA$

$f_2 = AB\overline{C} + A\overline{B}C + \overline{A}BC$

7 What is meant by simulation? Explain in detail about switch level and circuit level simulation?

8 (a) What is a Fault Model? Explain in detail about Stuck at Fault Model?

(b) Explain the terms Fault simulation, Fault coverage and Fault collapsing.

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