Code: 9A04605

R09

B.Tech III Year II Semester (R09) Supplementary Examinations December/January 2015/2016

VLSI DESIGN

(Common to ECE, EIE and E.Con.E)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) What is SOI process? Explain clearly about the advantages and disadvantages of it.
(b) Write about floating body voltage.

2 (a) Explain the Tunneling mechanism in MOS devices.
(b) How does the transistor characteristics are influenced by the temperature?

3 Design a layout diagram for two input NMOS NOR gate.

4 (a) Realize the logic function $[(AB)+(CD)]'$ using compound gates.
(b) Realize the logic function $x_1'+ x_2' x_3'$ using compound gates.

5 (a) Write about switch logic and hence compare the properties of pass transistor and transmission gate used as switches in NMOS and CMOS respectively.
(b) Implement 8:1 multiplexers using CMOS switch logic.

6 (a) Explain about the designing of a chip with sea of gates (SOG).
(b) Write about FPGA.

7 What is meant by logic synthesis? Explain in detail the advantages and disadvantages of network restructuring in order to obtain logic optimization.

8 (a) Differentiate between chip level test techniques and system level techniques.
(b) Explain any one of the chip level and system level methods.

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