Code: 9A05704 **R09**

B.Tech III Year II Semester (R09) Supplementary Examinations December/January 2015/2016

ADVANCED COMPUTER ARCHITECTURE

(Computer Science & Systems Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain Flynn's classification of various computer architectures.
(b) With a neat block diagram, explain the uniform memory access (UMA) multiprocessor model.

2 (a) What are the grand challenges that revel the opportunities for massive parallelism?
(b) Discuss the basic metrics affecting the scalability of a computer system for a given application.

3 (a) Describe the functional modules and physical limitations of backplane bus specification.
(b) Explain in detail about the Collision-Free scheduling.

4 Explain briefly about the message formats and various message routing schemes in multicomputer network.

5 (a) Explain briefly six types of vector instructions in vector processor.
(b) Discuss how the inter-processor communication is built in CM-5.

6 (a) What are implementation and management issues of shared virtual memory? Explain.
(b) Explain four parameters defined to analyze the performance of multithreaded massive parallel processing systems.

7 (a) What are the basic design issues in instruction level parallelism? Discuss.
(b) Explain in detail about the register renaming.

8 (a) Describe briefly about the semiconductor technology.
(b) Differentiate structural parallelism versus instruction level parallelism.

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