

SS**Code: 9A04605**

B.Tech III Year II Semester (R09) Supplementary Examinations December/January 2015/2016

VLSI DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours

Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

- 1 What are the four major CMOS technologies? Explain any one with flow chart.
- 2 (a) Draw the circuit of nMOS inverter and explain its operation. Draw and explain its transfer characteristics.
(b) Determine the pullup up to pull down ratio for an nMOS inverter driven by another nMOS inverter.
- 3 Draw the CMOS 2 input NAND gate, its physical lay out with its stick diagram.
- 4 Calculate gate capacitance value of 2 μm technology minimum sized transistor with gate to channel capacitance value of $8 \times 10^4 \text{ pF/ohm } \mu\text{m}^2$.
- 5 Explain the following terms with respect to C-MOS design:
 - (a) Structured design.
 - (b) Hierarchy.
 - (c) Regularity.
 - (d) Modularity.
 - (e) Locality.
- 6 (a) Write about standard cell based design
(b) Implement an optimized 3X8 binary decoder using PLA
- 7 (a) Give the Behavioral and Structural description of JK flip-flop in VHDL
(b) Give the Behavioral and Structural description of Full adder in VHDL? And implement the design using PLA.
- 8 Write about Design for Testability? And hence discuss in detail about the need for it in VLSI
