Code: 13A04303



B.Tech II Year I Semester (R13) Supplementary Examinations June 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: $(10 \times 02 = 20 \text{ Marks})$
 - What is the BCD equivalent of 456? (a)
 - (b) Draw the logic symbols of NAND and NOR gates.
 - Write the advantages of Tabulation method over K-Map method. (c)
 - Write the given Boolean expression f = A+B in Sum of minterms. (d)
 - Define combinational logic design. (e)
 - Define the Decoder. (f)
 - Write the difference between Latch and Flip flop. (g)
 - List asynchronous inputs of a sequential device. (h)
 - List out list of PLDs. (i)
 - Write the difference between RAM and ROM. (j)

PART - B

(Answer all five units, $5 \times 10 = 50 \text{ Marks}$)

UNIT – I

2 Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent.

OR

- 3 Perform the following:
 - (i) Subtraction by using 10's complement for the given 3456 245.
 - (ii) Subtraction by using 2's complement for the given 111001-1010.

UNIT -IN

Minimize the following Boolean function using k-map and realize using NAND Gates F(A, B, C, D)= 4

 $\Sigma m(0, 2, 4, 6, 8, 10, 12, 14).$

Minimize the given Boolean function $F(A,B,C,D) = \sum m(0,1,2,3,6,7,13,15)$ using tabulation method and 5

implement using basic gates.

- Design 8X1 Multiplexer by using 4X1 Multiplexers. 6 (a)
 - (b) Implement half adder using Decoder.

OR

Design a 4 bit adder cum subtractor using 1 bit full adders and explain. 7

UNIT – IV

- Design D Flip Flop by using SR Flip Flop and draw the timing diagram. 8 (a)
 - (b) Write the differences between combinational and sequential circuits.

OR

- Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop. 9 (a)
 - Design T Flip Flop by using JK Flip Flop and draw the timing diagram. (b)

UNIT – V

- Define asynchronous sequential design. 10 (a)
 - Implement the following Boolean functions $F_1 = \Sigma$ m (0, 1, 2, 3, 8, 10, 12, 14), $F_2 = \Sigma$ (0, 1, 2, 3, 4, 6, 8, (b) 10.12, 14) using PAL.

Draw and explain the construction of 4X3 RAM