

Code: 9A04306

**R09** 

B.Tech II Year I Semester (R09) Supplementary Examinations June 2016

## **DIGITAL LOGIC DESIGN**

(Computer Science & Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions All questions carry equal marks

\*\*\*\*

- 1 (a) Apply the number conversions from one system to other using its base:
  - (i)  $(344.25)_{10} = ()_2$ .
  - (ii)  $(1001110.01)_2 = ()_{10}$ .
  - (iii) (CDEF)<sub>16</sub> = ()<sub>2</sub>.
  - (iv)  $(572)_8 = ()_{16}$ .
  - (b) Given the binary numbers X = 1110110 and Y = 1100010. Perform the subtraction X-Y and Y-X using complements.
- 2 (a) Realize basic logic gates using Universal gates.
  - (b) Simplify the following expression Y = (A+B)(A+C')(B'+C').
- 3 Simplify the following Boolean function, using five variable maps:

$$F(A,B,C,D,E) = \Sigma(0,1,4,5,16,17,21,25,29)$$

- 4 (a) Design a 4-bit adder-subtractor circuit and explain the operation in detail.
  - (b) Design a 4x1 multiplexer and explain the working.
- 5 Explain the working of the following:
  - (a) J-K flip-flop.
  - (b) S-R flip-flop.
  - (c) D-flip-flop.
- 6 Explain the design of a 4-bit binary counter with parallel load in detail.
- 7 Design a combinatorial circuit using ROM and PLA. The circuit accepts 3-bit number and generates output binary number equal to square of input number.
- An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are:

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1.$$

$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1.$$

 $Z = x_2 + y_1$ .

Implement the circuit defined above with NAND SR latches.

\*\*\*\*