Code: 13A04303 **R13/SS**

B.Tech II Year II Semester (R13) Regular & Supplementary Examinations May/June 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Find the values of a & b in given expression $1776_{10} = a_8 = b_2$.

(b) In the following series, the same integer is expressed in different number systems. Determine the missing member in the series $10000, 121, 100, ?, 24, 22, 20, \ldots$.

(c) Does the given: (i) 1110. (ii) 0111 represent valid BCD codes?, if not represent in BCD codes.

(d) List out differences between Edge-triggering and Level-triggering.

(e) Explain the terms encoder and priority encoder.

(f) Explain the concept of OR gate.

(g) List out Operating characteristics of Flip-Flops.

(h) Clearly differentiate latch, flip-flop and memory.

(i) Explain the terms: (i) Static RAM. (ii) Dynamic RAM.

(j) Differentiate the terms: (i) Synchronous and asynchronous. (ii) Combinational and sequential.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Obtain the canonical and standard forms of given function $f_1 = (\mathrm{AB'(C + BD)} + \mathrm{A'B')C}$.

(b) Explain the concept of weighted and non-weighted codes with examples.

OR

3 (a) Explain the concept of reflection of gray codes.

(b) Implement and realize the given function $f_2 = \big((AB + \bar{C})D + EF\big)$using NAND gates only.

UNIT – II

4 (a) Using a K-map convert the given expression into: (i) minimum POS. (ii) standard SOP.
$f_3 = (A' + B' + C + D)(A + B' + C + D)(A + B + C + D')(A + B + C' + D)(A' + B + C + D')(A + B + C' + D)$?

(b) Define prime implicant With the aid of K-map. Obtain prime implicants for the functions:
(i) $f_4(x, y, z) = \sum(0,1,6,7)$.
(ii) $f_5(w, x, y, z) = \sum(0,1,2,3,4,8,11) + \Phi(6,9,10)$.

OR

5 (a) Use the tabulation procedure to generate set of prime implicants and to obtain the minimal expression for the function $f_6(v, w, x, y, z) = \sum(0, 1, 3, 8, 9, 13, 14, 15, 16, 17, 19, 24, 25, 27, 31)$.

(b) Minimize the given function $f_7 = \sum(1, 5, 6, 12, 13, 14) + \emptyset(2, 4)$. Hence implement using NOR gates only.

UNIT – III

6 (a) Design and Realize BCD to seven segment decoder using NAND gates only.

(b) Design and Realize a full adder using two half adders and logic gates.

OR

7 (a) Design and Realize $f_8 = \prod(0,1,3,7,9,10,11,13,14,15)$ using 8:1 mux.

(b) Design and Realize a full subtractor using NAND logic gates.

Contd. in page 2

Code: 13A04303 **R13/SS**

UNIT – IV

8 (a) Design and write the analysis of NOR gate SR latch.

(b) Design and Realize the conversion of JK flip-flop to: (i) D flip-flop. (ii) T flip-flop hence mention the differences.

OR

9 (a) What are the functions of a register and explain about parallel-in and parallel-out shift registers in detail using D FF's?

(b) Design and Realize a counter that can count states 0,1,2,3,4,5,6 using D-Flip flop.

UNIT – V

10 (a) Explain about the static hazard and show how it can be removed for the expression $f_9(x, y, z) = \sum(2,3,5,7)$.

(b) Design the state diagram for a two-input, two-output synchronous circuit that produces 1 whenever 0101 sequence occurs.

OR

11 (a) Draw the block diagram and explain in detail about the PAL.

(b) Realize $f_{10} = \sum(0, 1, 3, 5, 7, 9, 11, 13, 14, 15)$ using PLA.

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