

R09**Code: 9A04404****B.Tech II Year II Semester (R09) Supplementary Examinations May/June 2016****PULSE & DIGITAL CIRCUITS**

(Common to EIE, E.Con.E, ECE, ECC & MCT)

Time: 3 hours

Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

- 1 (a) Prove that for any periodic input wave form the average level of the steady state output signal form the RC high pass circuits is always zero.
(b) Prove the above statement for different periodic input waveforms.
- 2 (a) Explain synchronized clamping circuit.
(b) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.
- 3 (a) Explain with relevant diagram the various transistor switching times.
(b) Explain the storage and transition times of the diode as a switch.
- 4 (a) Explain how a Schmitt trigger can be used as a comparator and as a squaring circuit.
(b) What do you understand by hysteresis? What is hysteresis voltage? Explain how hysteresis can be eliminated in a Schmitt trigger.
- 5 (a) What is the effect of recovery interval on the sweep output?
(b) How do you get minimum recovery time in a bootstrap time base circuit?
(c) Define slope speed error and transmission error.
- 6 (a) What are the draw backs of two diode sampling gate?
(b) Write about different capacitances which effect on the operation of sampling gates?
- 7 (a) Explain the phenomena of phase delay in one shot circuits.
(b) How frequency division is related with synchronization? Explain.
- 8 (a) With a neat circuit diagram, explain the operation of ECL NOR gate.
(b) Calculate noise margin for a standard ECL gate.
