R09

Code: 9A04504

B.Tech III Year I Semester (R09) Supplementary Examinations June 2016

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Design a CMOS transistor circuit that has the functional behavior: $f(Z) = \overline{A.(B+C)}$.

(b) Design a 4-input CMOS AND-OR-INVERT gate? Draw the logic diagram and function table.

2 (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior.

(b) Mention the DC noise margin levels of ECL 10K family.

3 (a) Design a logic circuit to detect prime number of a 5-bit input.

(b) Write the structural VHDL program for the above design.

4 (a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram.

(b) Explain the structural design elements of VHDL.

5 What is 74X138? Give the logic symbol for 74X138 and write a VHDL code in structural model.

6 Write a VHDL code for 8 bit comparator circuit. Using this entity write a VHDL code for 24 bit comparator. Use the structural model for it.

7 Explain the operation of a 4 bit synchronous binary counter with the required diagram and wave forms.

8 (a) Draw and explain the internal structure of a 128X1 ROM using two dimensional decoding.

(b) Explain the detail view of internal structure of ROM with a good example.

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