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Code: 9A04605 **R09**

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2016

VLSI DESIGN

(Common to ECE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

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1 (a) Why is NMOS technology more preferred than PMOS technology?
(b) Compare CMOS and BI-CMOS technology.

2 (a) Explain the electrical properties of MOS transistor in detail.
(b) Derive an expression for V_{in} of a CMOS inverter to achieve the condition $V_{in} = V_{out}$. What should be the relation for $\beta_n = \beta_p$?

3 (a) Derive the expression for rise time, fall time and propagation delay of CMOS inverter.
(b) What is MOS scaling? Explain scaling models in detail.

4 (a) Explain commonly used techniques to estimate the delay time of a MOS inverter.
(b) Draw the alternate gate circuits CMOS inverter.

5 (a) Explain the structural design of 4x1 multiplier.
(b) Construct a transmission gate full adder circuit.

6 (a) Write the differences between FPGA and CPLD.
(b) Implement full adder using PAL.

7 (a) Write the VHDL code for full adder.
(b) Explain blocking & non-blocking statements.

8 (a) Design the principal and application of BST.
(b) Write about sequential logic testing.

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