Code: 9A04704 **R09**

B.Tech IV Year I Semester (R09) Supplementary Examinations June 2017

DSP PROCESSORS & ARCHITECTURES

(Common to ECE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) With necessary block diagram, explain multiply and accumulate unit.
(b) With necessary examples, explain circular addressing and bit reversed addressing modes.

2 (a) What is fixed point format? What is the range of numbers that can be represented in a fixed point format using 16 bits if the numbers are treated as signed integers?
(b) Explain different sources of error in DSP implementations.

3 (a) With necessary sketches, explain bus architectures for Von Neumann and Harvard Architectures.
(b) Explain the functions of address generation unit.

4 (a) Explain pipeline operation of TMS320C54XX processors.
(b) With necessary example, explain branch instructions B & BACC.

5 (a) What is Q-notation? What values are represented by the 16-bit fixed point number N = 4000 h in the Q15 and the Q17 notations?
(b) Write a TMS320C5XX program to multiply two Q15 numbers.

6 (a) Explain the 8-point FFT implementation on TMS320C54XX.
(b) State the importance of bit reversed index generation.

7 (a) Explain memory space organization of TMS320C5416.
(b) Discuss memory interface for the TMS320C5416 processor.

8 (a) With necessary flow graphs, explain the FPGA based DSP system design.
(b) Give a comparative note on systems designed using FPGAs and DSPs with necessary illustrations.

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