Code: 9A04706 **R09**

B.Tech IV Year I Semester (R09) Supplementary Examinations June 2017

DIGITAL DESIGN THROUGH VERILOG HDL

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

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1 Explain briefly about:
(a) Simulation and synthesis.
(b) System tasks.
(c) Programming language interface module.

2 (a) Write a gate level verilog program to realize a full adder using half adders and an OR gate.
(b) What are the various types of delays associated with gate level modeling and explain how these delays can be represented in HDL.

3 (a) Describe the procedural assignments with suitable examples.
(b) Write a verilog code for up-down counter in behavioral modeling using for loop statement.

4 (a) Explain the operators in verilog HDL and their precedence in detail with suitable examples.
(b) Explain time delays associated with switch primitives.

5 (a) Distinguish between system tasks and functions.
(b) Explain the syntax for the function declaration and invocation.

6 (a) Explain the implementation procedure of the dice game using state machine chart.
(b) Explain the linked state machines in detail.

7 (a) Explain the architecture of XILINX FPGA architecture in detail.
(b) Discuss the configuration of CLB in XC3000.

8 (a) Write a verilog model of static SRAM memory.
(b) Explain the procedure of interfacing memory to microprocessor bus.

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