Code: 13A05709 **R13/SS**

B.Tech IV Year I Semester (R13) Supplementary Examinations June 2017

ADVANCED COMPUTER ARCHITECTURE

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Define turnaround time and system throughput.
(b) Define Latency with example.
(c) Explain memory bound problem.
(d) What is the need of Arbiter and Interrupter modules?
(e) Explain the problem of clock skewing.
(f) Describe centralized network control strategy.
(g) Define vector processor.
(h) What is vector loop? How vector segmentation is done?
(i) Define page swapping.
(j) Draw an example dataflow graph.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Explain about the Flynn's classification of computer architectures.
(b) List and explain five types of Data Dependency.

OR

3 With a neat block diagram, explain the architecture of a Vector Supercomputer.

UNIT – II

4 (a) What are the important characteristics of parallel algorithms which are machine implementable? Explain.
(b) Explain about the basic metrics affecting the scalability of a computer system.

OR

5 Illustrate about speedup performance model, Amdahl's law for a fixed workload.

UNIT – III

6 (a) Explain synchronous pipeline model with suitable diagram.
(b) Discuss in detail about blocking and non blocking networks.

OR

7 Describe Tomasulo algorithm for dynamic instruction scheduling in detail with suitable example.

UNIT – IV

8 (a) With a neat diagram, explain the C/S-Access Memory Organization.
(b) Give a brief note on compound vector functions.

OR

9 With a neat block diagram, explain the architecture of the Connection Machine CM-2.

UNIT – V

10 (a) Describe Prefetching techniques and their benefits.
(b) Give a brief note on Tera Multiprocessor design goals.

OR

11 Illustrate multithreaded architecture and its computation model for a massively parallel processing system.

*****