Code: 9A04306

R09

B.Tech II Year I Semester (R09) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN

(Computer Science & Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the principle of basic logic gates with neat sketches and truth tables.
(b) Convert the following:
(i) $(48)_{10} = (\ )_2 = (\ )_8 = (\ )_{16}$.
(ii) $(121)_8 = (\ )_{10} = (\ )_{16} = (\ )_2$.

2 (a) Write the axiomatic definitions of Boolean algebra.
(b) State and prove De-Morgan's laws.
(c) Explain canonical and standard forms of Boolean algebra. Convert x' + yz into canonical form.

3 (a) Reduce the following expression using K-Map and realize it with NAND gates:
$F(A,B,C,D) = \sum m(4,5,8,9,11,12,13,15)$
(b) Implement: (i) AND. (ii) OR. (iii) NOT gates by NAND gates only.

4 (a) What is a combinational circuit? Explain with one example.
(b) Design a full adder with two half adders and OR gate.

5 (a) What is a latch and flip-flop?
(b) Mention the applications of flip-flops.
(c) Explain master-slave JK-flip flop with characteristic table.

6 (a) Explain the terms PRESET and CLEAR with relevant tables.
(b) What is Ripple counter?
(c) Design a MOD-10 (Decade) synchronous counter.

7 (a) What is meant by memory expansion? Explain its limits.
(b) Differentiate static and dynamic RAM.
(c) Explain in detail about ROM and types of ROM.

8 (a) What is an asynchronous sequential circuit? Explain the design procedure.
(b) What is a hazard in asynchronous sequential logic? Explain different types of hazards.

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