Code: 9A12301

R09

B.Tech II Year I Semester (R09) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN & COMPUTER ORGANIZATION

(Common to CSS & IT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) What is an error detection code? Write about error detection codes by giving examples.
(b) Convert the following numbers to decimal.
(1001001.011)2, (12121)3, (1032.2)4, (4310)5, (0.342)6 (50)7, (8.3)9, (198)12

2 (a) Design a 4-bit ring counter using D-Flip-flops and draw the circuit diagram and timing diagrams.
(b) Design a D-type positive edge triggered flip flop. Also show the operation of the sequential circuit when CP = 1.

3 What is an universal shift register? What are its capabilities? Design a 4-bit universal shift-register that has all the capabilities.

4 (a) Indicate the computational details of multiplying two 4-bit numbers 1011 and 0101 using Booth's algorithm. Verify the result obtained.
(b) Give the basic features of the IEEE floating point number standard.

5 (a) With the help of diagram, explain about interrupt cycle execution.
(b) Explain about IA-32 architecture supported addressing modes with examples.

6 (a) Explain how a word can be fetched from the memory using timing signals.
(b) Explain the implementation of one-bit register with a neat diagram.

7 (a) Discuss the Internal structure of 64 X 1 DRAM with help of a sketch.
(b) Explain the Timing diagram of the READ and WRITE cycle of Dynamic RAM.

8 (a) Explain hardware controlled data transfer with the help of a block diagram.
(b) Discuss the limitations of programmed I/O and interrupt driven I/O. Explain hardware controlled data transfer.

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