Code: 13A04303 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations June 2017

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) If $143_5 + 341_5 = X_{10}$, then X is -----

(b) Implement Y = A + B C using minimum number of two input NAND gates.

(c) What is the importance of don't care condition?

(d) SOP of F(x, y, z)=∑(2, 3, 6, 7) is ----

(e) What is the function of magnitude comparator?

(f) What is the importance of prime implicants?

(g) What is the function of EAROM?

(h) Where Registers are used?

(i) Draw the logic circuit of flip-flop and truth table using NAND gates.

(j) A PLA is similar to ROM in concept? Yes or No? How? Why?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Convert the following to decimal and then to hexadecimal.

(i) 1234_8 (ii) 11001111_2

OR

3 Find the complement of the following Boolean function and reduce into minimum number of literals.

Y= BC'+A'D+DB'+CD'

UNIT – II

4 Using K-map method simplify the following switching function:

F(W,X,Y,Z)=∑m(0,1,4,5,6,7,9,11,15) + ∑d(10,14) and implement using NAND gates

OR

5 Simplify the following expression using tabulation method:

F(A,B,C,D,E)= ∑ (4,6,7,9,11,12,13,14,15,20,22,25,27,28,30)+d(1,5,29,31)

UNIT – III

6 Realize f = ∑m(0,1,2,5,6,7,9,12,15) using 4X1 multiplexer.

OR

7 Realize 5-32 line decoder using multiple 3-8 line 74x138 decoders.

UNIT – IV

8 Draw the circuit of JK flip flop using NAND gates and explain its operation.

OR

9 Design a synchronous 3-bit up-down counter using JK flip flops.

UNIT – V

10 Realize f = ∑m(0,2,3,7,9,11,15,16) using ROM.

OR

11 Realize f = ∑m(0,2,4,5,7,9,11,15,16) using PLA.

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