B.Tech II Year I Semester (R13) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART - A

(Compulsory Question)

- 1 Answer the following: $(10 \times 02 = 20 \text{ Marks})$
 - (a) Reduce AB + (AC)' + AB'C (AB + C).
 - (b) Simplify the following expression Y = (A + B)(A + C')(B' + C').
 - (c) Define K-map? Name its advantages and disadvantages.
 - (d) Write about universal logic gates and realize XOR gate using Universal gates.
 - (e) Construct full adder using half adders.
 - (f) Compare a decoder with a Demultiplexer.
 - (g) What is race around condition?
 - (h) Write about bidirectional shift register.
 - (i) List basic types of programmable logic devices.
 - (j) Explain about parallel in serial out shift register.

PART - B

(Answer all five units, $5 \times 10 = 50 \text{ Marks}$)

UNIT – I

- 2 (a) Convert 1A53 Hexadecimal to its decimal equivalent.
 - (b) Convert (734)₈ to its hexadecimal equivalent.
 - (c) Convert 0.640625 decimal number to its octal equivalent
 - (d) Convert 0.1289062 decimal number to its hex equivalent

OR

3 Prove the following identities:

(i) A' B' C' + A' B C' + A B' C' + A B C' = C'.

(ii) A B + A B C + A' B + A B' C = B + A C

UNIT – II

- A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations a) A is False b) A, B, C are True
 - (i) Write the Truth table for F. Use the convention True = 1 and False = 0.
 - (ii) Write the simplified expression for F in SOP form.
 - (iii) Write the simplified expression for F in POS form.
 - (iv) Draw logic circuit using minimum number of 2-input NAND gates.

OR

5 Simplify the following expression into sum of products using Karnaugh map:

 $F(A, B, C, D) = \sum (1, 3, 4, 5, 6, 7, 9, 12, 13)$

UNIT – III

6 Draw and explain the working of a carry-look ahead adder.

OR

- 7 (a) Design a 4-bit adder-subtractor circuit and explain the operation in detail.
 - (b) Explain the functionality of a decoder.

Contd. in page 2

UNIT - IV

8 Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

OF

9 Define a register. Construct a shift register from S-R flip-flops. Explain its working.

UNIT – V

10 (a) Compare PLA with PROM.

(b) What is ROM? List the different types of ROMs.

OR

Write about the following:

- (a) CMOS logic.
- (b) Digital logic circuits.

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