



B.Tech II Year I Semester (R15) Supplementary Examinations June 2017

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE & EIE)

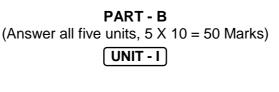
Time: 3 hours

Max. Marks: 70

PART - A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
 - (a) Convert $(AOCB, EE)_{16}$ into decimal number.
 - (b) Perform the subtraction (-6)-(-13) using signed 2's complement representation.
 - (c) Express F = A + B'C in sum of min-terms or SOP form.
 - (d) Implement OR gate using only NAND gates.
 - (e) Differentiate combinational and sequential circuits.
 - (f) What is encoder?
 - (g) Draw the circuit of ring counter.
 - (h) What are the differences between synchronous and asynchronous sequential circuits?
 - (i) Give the comparison between PLA and PAL.
 - (j) What is FPGA?



2 Convert the following:

(a) $AB_{16} = ()_{10}$ (b) $1234_8 = ()_{10}$ (c) $10110011_2 = ()_{10}$ (d) $772_{10} = ()_{10}$

(d) $772_{10} = ()_{16}$ (e) $(0.513)_{10} = ()_8$

OR

Write the following binary numbers in signed 1's complement form and signed 2's complement form using 16 bit registers.
(i) +1001010
(ii) -11110000
(iii) -11001100.1
(iv) +100000011.111

UNIT - II)

- 4 Simplify the following Boolean function using tabulation method. $Y(A, B, C, D) = \Sigma(1, 3, 5, 8, 9, 11, 15)$
- 5 Realize the following function using only 2-input NAND gates. F = A'BC' + BD + AC + B'C'D'.

UNIT - III

6 Explain how a decoder can be converted into a de-multiplexer with relevant block diagrams and truth tables.

OR

7 Draw and explain the XS-3 subtractor using 4 bit binary adders.

UNIT - IV

8 Explain hazards in sequential circuits.

OR

9 Convert D-flip flop into T, JK and SR flip flop.

UNIT - V

10 Describe DRAM with an appropriate diagram and explain about its timings.

OR

Tabulate the PLA programming table for the four Boolean functions listed below. $A(x,y,z) = \Sigma(1,2,4,6)$ B(x,y,z) www.FirstRankerzcon (2,6) $D(x,y,z) = \Sigma(1,2,3,5,7)$