

B.Tech II Year I Semester (R15) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN

(Common to CSE and IT)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- If $143_5 = X_6$, then X is ----
 - What is meant by binary logic?
 - Implement $Y = A + B C$ using minimum number of two input NAND gates.
 - What is the importance of prime implicants?
 - What is problem of lock out in counters? Explain.
 - What is the working principle of magnitude comparator?
 - What is meant by Flip-Flop?
 - Where the ripple counter is used? Explain.
 - What is the function of EAROM?
 - Draw the circuit diagram of TTL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- 2 Convert the following to Decimal and then to Octal. (i) 4204_{16} . (ii) 1010011_2 .

OR

- 3 Find the complement of the following Boolean function and reduce into minimum number of literals.
 $Y = (BC' + A'D)(DB' + CD')$

UNIT – II

- 4 Using 5-variable k-map, find minimal SOP expressions for the following logic function:

$$F = \sum(0, 2, 4, 5, 6, 7, 8, 10, 17, 18, 21, 29, 31) + d(11, 20, 22)$$

OR

- 5 Simplify the following expression using tabulation method:

$$F(A, B, C, D, E) = \sum(0, 1, 2, 3, 4, 5, 10, 11, 14, 20, 21, 24, 25, 26, 27, 28, 29, 30)$$

UNIT – III

- 6 Design 32:1 Multiplexer using two 16:1 Multiplexers and one 2:1 Multiplexer.

OR

- Design a 4 bit binary-to-BCD code converter.
- Briefly explain the operation of a carry look ahead adder

UNIT – IV

- Design and draw the logic diagram for MOD-6 ripple counter.
- How is the race around condition eliminated in JK Flip Flop?

OR

- 9 Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.

UNIT – V

- Explain about MOS and CMOS logic.
- Explain about basic circuit and NOR of ECL with its characteristics.

OR

- Write short notes on PLA.
- Implement the following Boolean function using PLA:

$$F_1(A, B, C) = \sum m(3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum m(0, 2, 4, 7)$$
