Code: 9A04401

# B.Tech II Year II Semester (R09) Supplementary Examinations May/June 2017 <br> SWITCHING THEORY \& LOGIC DESIGN <br> (Common to EEE, EIE, E.Con.E, ECE \& ECC) 

Time: 3 hours
Max. Marks: 70
Answer any FIVE questions
All questions carry equal marks
1 (a) Explain 7-bit Hamming code.
(b) A receiver with even parity Hamming code is received the data as 1101101. Determine the correct code.

2 (a) State and prove Boolean laws related to OR, AND, NOT gates.
(b) Determine the canonical sum of products form of the following function.

$$
f(x, y, z)=z+\left(x^{\prime}+y\right)\left(x+y^{\prime}\right)
$$

(c) Realize XOR gate using minimum number of NAND gates.

3 (a) What are the advantages of Tabulation method over K-map?
(b) Simplify the following Boolean function using Tabulation method.

$$
Y(A, B, C, D)=\sum(0,1,3,4,5,6,11,13,14,15)
$$

4 (a) What is Encoder? Design decimal to BCD Encoder.
(b) Implement Full Subtractor using decoder and OR gates.

5 (a) Write short notes on combinational logic implementation using ROM.
(b) Derive a PLA programming table for the combinational circuit that squares a 3 bit number.

6 (a) What are asynchronous inputs in flip-flops? Explain its functionality.
(b) With neat sketch, explain JK master slave flip-flop.

7 (a) What are the capabilities and limitations of Finite State Machine?
(b) Find the equivalence partition and a corresponding reduced machine in standard form.

| PS | $\mathrm{NS}, \mathrm{Z}$ |  |
| :---: | :---: | :---: |
|  | $\mathrm{X}=0$ | $\mathrm{X}=1$ |
| A | $\mathrm{E}, 0$ | $\mathrm{C}, 0$ |
| B | $\mathrm{C}, 0$ | $\mathrm{~A}, 0$ |
| C | $\mathrm{B}, 0$ | $\mathrm{G}, 0$ |
| D | $\mathrm{G}, 0$ | $\mathrm{~A}, 0$ |
| E | $\mathrm{F}^{\prime}, 0$ | $\mathrm{~B}, 0$ |
| $\mathrm{~F}^{\prime}$ | $\mathrm{E}, 0$ | $\mathrm{D}, 0$ |
| G | $\mathrm{D}, 0$ | $\mathrm{G}, 0$ |

8 (a) Explain the symbols used in an ASM chart with neat diagrams.
(b) Explain the important features of the ASM chart.

