

Code: 9A04404

B.Tech II Year II Semester (R09) Supplementary Examinations May/June 2017

PULSE & DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC & MCT)

Time: 3 hours

Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

- 1 (a) Explain the response of a high pass circuit when an exponential input is applied.
(b) Write short note on piping process.
- 2 (a) Explain transfer characteristics of the emitter coupled clipper and derive the necessary equations.
(b) Discuss the applications of voltage comparator.
- 3 (a) Explain the phenomenon of latching in a transistor.
(b) Write short note on junction swing times.
- 4 (a) Design a collector coupled transistor monostable multivibrator to produce a time delay of 100 μ sec. Use transistors having h_{FE} of 250. Use ± 12 V sources, $V_{CE(sat)} = 0.3$ V, $V_{BE(sat)} = 0.7$ V and $V_{BE(cutoff)} = 0$ V.
(b) Show that the astable multivibrator works as voltage controlled oscillator.
- 5 What is meant by time base? What is its role in CRO? Why it should be linear?
- 6 (a) Why are sampling gates called selection circuits?
(b) What are the advantages of unidirectional sampling gates?
- 7 (a) Explain the generation of saw tooth waveform using RC sweep circuits.
(b) What are the factors that affect the phase delay?
- 8 (a) List various characteristics of logic families.
(b) Explain the concepts: (i) Open collector. (ii) Tristate outputs.
