Code: 13A05401 **R13**

B.Tech II Year II Semester (R13) Supplementary Examinations May/June 2017

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to IT & CSE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define the following: (i) Computer organization. (ii) Computer architecture.
(b) List the basic types of operations that are needed to be supported by an instruction set.
(c) What is an addressing mode? List addressing modes.
(d) List the different factors considered while designing an I/O subsystem.
(e) How is hard-wired control different from micro-programmed control?
(f) What is cache coherence problem? List the approaches to maintain consistent multi cache copies.
(g) Write the procedure to handle an interrupt.
(h) What is the purpose of hardware interlock in data dependency conflict?
(i) Write the characteristics of multiprocessors.
(j) What is pipelining? Why do we use it?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain about I/O subsystem organization with neat diagrams.

OR

3 Describe simple computer levels of programming languages.

UNIT – II

4 What is instruction cycle? Draw and explain about instruction cycle with flow chart.

OR

5 Explain the rules for basic architecture operations of floating point numbers.

UNIT – III

6 Explain the basic organization of a micro programmed control unit and the generation of control signals using micro program.

OR

7 Describe the design of control unit.

UNIT – IV

8 Analyze memory hierarchy in terms of speed size and cost.

OR

9 Explain the functions of a typical 8-bit parallel interface in detail.

UNIT – V

10 Explain the interprocess communication mechanism in CM-5.

OR

11 Describe the system free structure for multiprocessors.

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