Code: 15A05402 **R15**

B.Tech II Year II Semester (R15) Regular Examinations May/June 2017

COMPUTER ORGANIZATION

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What are the two possibilities of increasing the clock rate?
(b) Define register mode with example.
(c) Describe the configuration of n-bit ripple-carry adder.
(d) Define control word.
(e) List the advantages of using cache memory.
(f) Define access time.
(g) What are vectored interrupts?
(h) List two key objectives of universal serial bus.
(i) What is the use of pipelining?
(j) Draw an example 3-dimentional hypercube network.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) What is system software? What are the various functions performed by system software?
(b) Describe indirect addressing mode with suitable examples.

OR

3 Draw the basic functional unit of computer and explain each unit in detail.

UNIT – II

4 (a) Assuming 6-bit 2's-complement number representation, multiply the multiplicand A = 110101 by the multiplier B = 011011 using the normal Booth algorithm.
(b) Draw the basic structure for data processing unit and discuss in detail about it.

OR

5 Illustrate Bit-Pair recoding of multipliers derived form Booth recoding with example.

UNIT – III

6 (a) Suppose that a computer has a processor with two L1 caches, one for instructions and one for data and an L2 cache. Let τ be the access time for the two L1 caches. The miss penalties are approximately 15τ for transferring a block from L2 to L1, and 100τ for transferring a block from the main memory to L2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L1 and L2 caches are 0.96 and 0.80, respectively.
(i) Suppose that the L2 cache has an ideal hit rate of 1. By what factor would this reduce the average memory access time as seen by the processor?
(ii) Consider the following change to the memory hierarchy. The L2 cache is removed and the size of the L1 caches is increased so that their miss rate is cut in half. What is the average memory access time as seen by the processor in this case?
(b) What are the advantages and applications of flash memories?

OR

7 Describe virtual-memory address-translation method based on the concept of fixed-length Pages with a neat block diagram.

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UNIT – IV

8 Describe the use of DMA controllers in a computer system with a neat block diagram.

OR

9 Define interrupt? Illustrate the transfer of control through the use of interrupts.

UNIT – V

10 (a) Define hazard? Explain in detail about data hazards.
(b) Describe the general classification of parallel processing systems.

OR

11 Illustrate three possible ways of implementing a multiprocessor system with neat diagrams.

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