Code: 15A04302 **SS**

B.Tech II Year II Semester (R15) Regular Examinations May/June 2017

SWITCHING THEORY & LOGIC DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Convert $(0.51\ 5)_{10}$ to octal.

(b) What you mean by weighted code?

(c) What are the universal gates? Why they are called universal gates?

(d) Find the minterm expansion of f(a, b, c, d) = a'(b' + d) + acd'.

(e) Explain binary subtractor.

(f) What are the applications of multiplexers?

(g) Write the differences between Latches and flip flops?

(h) Draw the circuit of Johnsons counter.

(i) Write the classification of semiconductor memories?

(j) Give the comparison between ROM and PROM.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Why are complements used in binary arithmetic? What are the advantages and disadvantages of using 2s complement notation in binary arithmetic?

OR

3 Convert the following numbers as indicated:

(i) $(4350)_5 = (\ )_2$

(ii) $(11010011)_2 = (\ )_{16}$

(iii) $(552)_6 = (\ )_8$

(iv) $(1001001.011)_2 = (\ )_{10}$

(v) $(2AC5.D)_{16} = (\ )_{10}$

UNIT – II

4 Simplify the following Boolean expressions to a minimum number of literals:

(a) A'C' + ABC + AC'.

(b) (A' + C) (A' + C') (A + B + C'D).

OR

5 Simplify the following Boolean function to a minimum number of literals. F (A, B, C) = ∑(1, 4, 5, 6, 7). Draw the Logic diagram using NAND gates.

UNIT – III

6 Design a 4-bit comparator using four 1-bit comparator modules.

OR

7 Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer (use only block diagram).

UNIT – IV

8 Draw the logic diagram of a JK flip flop and using excitation table, explain its operation.

OR

9 Convert T-flip flop into D, JK and SR flip flop.

UNIT – V

10 Implement the following Boolean functions using a PAL that has four sections with three product terms each: F_1 (A, B, C, D) = ∑(2, 12, 13) and F_2 (A, B, C, D) = ∑(7, 8, 9, 10, 11, 12, 13, 14, 15).

OR

11 Given a 32 x 8 ROM chip with an enable input, show the external connection necessary to construct a 128 x 8 ROM with four chips and a decoder.

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