# B.Tech III Year I Semester (R09) Supplementary Examinations June 2017 SWITCHING THEORY \& LOGIC DESIGN 

(Mechatronics)
Time: 3 hours
Max. Marks: 70
Answer any FIVE questions
All questions carry equal marks

1 A receiver with even parity hamming code receives the data 1110110. Determine the correct code.
(a) Convert the given expression into canonical SOP form;
(i) $f=A B+B C+C A$
(ii) $f=A+A B+A B C$.
(b) $F(A, B, C, D)=\bar{B} D+\bar{A} D+B D$ express them as SOP and POS forms.

7 Determine the minimal state equivalent of the state table given below using partition technique. Also determine the minimum length of sequence that distinguishes state B from state C .

| PS | $\mathrm{NS}, \mathrm{Z}$ |  |
| :---: | :---: | :---: |
|  | $\mathrm{X}=0$ | $\mathrm{X}=1$ |
| A | $\mathrm{A}, 0$ | $\mathrm{E}, 1$ |
| B | $\mathrm{A}, 1$ | $\mathrm{E}, 1$ |
| C | $\mathrm{B}, 1$ | $\mathrm{~F}, 1$ |
| D | $\mathrm{B}, 1$ | $\mathrm{~F}, 1$ |
| E | $\mathrm{C}, 0$ | $\mathrm{G}, 0$ |
| F | $\mathrm{C}, 0$ | $\mathrm{G}, 0$ |
| G | $\mathrm{D}, 0$ | $\mathrm{H}, 0$ |
| H | $\mathrm{D}, 0$ | $\mathrm{H}, 0$ |

Obtain minimal SOP expression for the logic function $F=\operatorname{\Sigma m}(0,1,2,4,5,6,8,9,12,13,14)$ using K-map and realize using NOR gates.

Design a combinational logic circuit for BCD-to-seven segment decoder.

Implement the given functions using PAL:
(i) $Y_{0}=A B C D$.
(ii) $Y_{1}=\bar{A} \cdot B \cdot \bar{C}+A B C+A C+A B \bar{C}$
(iii) $Y_{2}=\bar{A} B C \bar{D}+\bar{A} B C D+A B C D$
(iv) $Y_{3}=\bar{A} B C \bar{D}+\bar{A} B C D+A B C D+A B C \bar{D}$

Design a 3-bit synchronous counter.

Obtain the ASM charts for the following state transitions:

If $X=1$, control goes from $T_{1}$ to $T_{2}$ and then to $T_{3}$. If $X=0$ control goes from $T_{1}$ to $T_{3}$.

