Code: 9A04504

R09

B.Tech III Year I Semester (R09) Supplementary Examinations June 2017

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate?

(b) Explain the behavioral difference between simple transistor logic inverter and Schottky logic inverter.

2 (a) Draw the circuit diagram of basic TTL NAND gate and explain three parts with the help of functional operation.

(b) Discuss the steps in VHDL design flow.

3 (a) What is the importance of time dimension in VHDL and explain its function?

(b) Design the logic circuit and write a data-flow style VHDL program for the following function:

$F(X) = \Pi_{A,B,C,D}(1,4,5,7,9,13,15)$

4 (a) Design a logic circuit to detect prime number of a 5-bit input.

(b) Using two 74×138 decoders design a 4 to 16 decoder.

5 Draw the logic diagram, logic symbol of 74x245 octal 3- state trans-receiver and explain its operation.

6 Write a behavioral VHDL code to compare 16 bit signed and unsigned integers and draw logic diagrams for:

(a) 4-bit equality comparator.

(b) 4-bit magnitude comparator.

7 (a) Distinguish between the synchronous and asynchronous counters.

(b) Design a mod-60 counter using 74 X 163 IC's.

8 Design a 4 X 4 unsigned multiplier using 256 X 8 ROM.

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