Code: 9A05406

R09

B.Tech III Year I Semester (R09) Supplementary Examinations June 2017

COMPUTER ORGANIZATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Discuss the interconnection structure design of a computer.
(b) Explain various bus lines.
(c) What do you mean by multiple-bus hierarchies?

2 (a) Discuss about logical and shift micro operations.
(b) What is stack? Explain push and pop instructions using stack.

3 (a) Explain the operation of micro program sequencer with neat diagram.
(b) Write micro-routines to fetch an instruction from memory.

4 (a) Explain in detail the array multiplier.
(b) With the help of a diagram, explain 2 bit by 2 bit array multiplier.

5 Explain with help of a sketch, the Internal structure of 64X1 DRAM.

6 (a) What is an interrupt? Discuss in detail single level interrupts and multi level interrupts.
(b) Draw a flowchart to explain the response to an interrupt.

7 (a) Explain the delayed branching and conditional branching.
(b) Discuss on interleaved memory organization.

8 (a) What do you mean by arbitration? Explain various techniques used for providing dynamic arbitration.
(b) Define multiprocessor system.

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