Code: 9A10504 **R09**

B.Tech III Year I Semester (R09) Supplementary Examinations June 2017

LINEAR & DIGITAL IC APPLICATIONS

(Common to E.Con.E, EIE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

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1 (a) Explain the dc and ac characteristics of an opamp.
(b) Define the terms CMRR, slew rate and PSRR for an opamp.

2 (a) Draw the circuit diagram of an instrumentation amplifier using opamp and explain its operation.
(b) Explain with diagram, the working of a V to I converter with grounded load.

3 (a) Draw the block diagram of a phase locked loop and explain the principle of operation and function of each block.
(b) Explain the application of a PLL for frequency multiplication.

4 (a) Summarize the characteristic features of CMOS logic family.
(b) Explain the CMOS steady state electrical behavior.

5 (a) Draw the working of a basic TTL logic circuit and explain its working.
(b) Explain the interfacing of CMOS and TTL logic circuits.

6 (a) Describe the various statements used in behavioral modeling of VHDL.
(b) Explain the use of tasks and functions of VHDL.

7 (a) Explain the design of a 8 bit unsigned adder in VHDL.
(b) Explain the design of m by n decoder with its implementation in VHDL.

8 Draw the state table, state diagram and logic circuit of a 1 digit decimal up counter and explain its implementation in VHDL.

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