B.Tech III Year I Semester (R09) Supplementary Examinations June 2017

DIGITAL SYSTEM DESIGN

(Computer Science & Systems Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Reduce the following state table to a minimum number of states.

Present state	Next state		Present
	X = 0	1	
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

(b) With an example, explain the use of ASM charts in the design of digital circuits.

2 (a) Design sequential comparator for binary numbers.

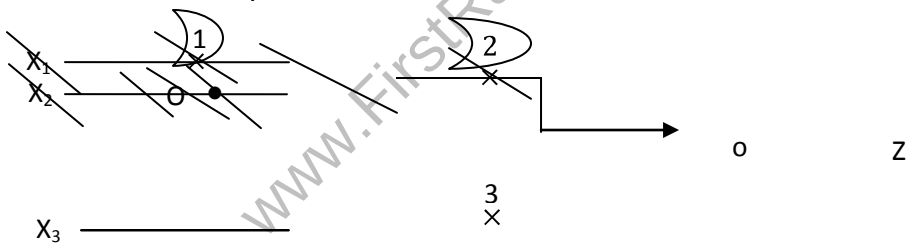
(b) Implement Mealy machine using CPLD.

3 (a) Discuss with examples Struck-at and bridging logic faults.

(b) What are the limitations of path sensitization and Boolean difference methods?

4 (a) Discuss different types of faults found in digital circuits. How can they be categorized?

(b) Using the path sensitization and Boolean difference method, find the test vectors for SA_0 and SA_1 fault on input line 1 and on the internal lines 2 and 3 of the circuit shown in figure.



5 (a) Explain the transition check approach of fault diagnoses in sequential circuits.

(b) Discuss the machine identification with respect to sequential circuits.

6 (a) Discuss in detail the column and row folding.

(b) Realize a three-bit adder by PLA: (i) Directly. (ii) By using complement carry.

7 (a) Explain the classification of PLA test methodologies.

(b) Discuss the deterministic test generation algorithm for PLAs.

8 (a) What are races? Discuss with examples, how to find a race-free assignment.

(b) Define critical race and noncritical race.

(c) With examples, explain two types of cycles.

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