Code: 13A04504 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations June 2017

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART - A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Give the logic levels and noise margins of CMOS and TTL families.
(b) Explain the term transition time with respect to CMOS logic.
(c) Discuss the binding between library and components.
(d) What are the structural design elements?
(e) Write a VHDL program for 4x1 multiplexer.
(f) Write a test bench for two input XOR gate using VHDL.
(g) Convert a T flip-flop into D flip-flop.
(h) What are the differences between PLA and PAL?
(i) Distinguish between SRAM and DRAM.
(j) List out the applications of ROM.

PART - B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Explain the following terms with reference to CMOS logic.
(i) Logic '0' and logic '1'.
(ii) Noise margin.
(iii) Power supply rails.
(iv) Propagation delay.

(b) Implement the following logic expression with CMOS AOI logic and explain its operation with the help of functional table.

$$Y = \overline{AB} \cdot \overline{CD}$$

OR

3 (a) Draw the circuit diagram of two input 10K ECL OR/NOR gate and explain its function with the help of truth table.

(b) What is interfacing? Explain interfacing between low voltage TTL and low voltage CMOS logic.

UNIT - II

4 Design the logic circuit and write a data-flow style VHDL program for the following functions.
(i) $f(A) = \Sigma\, p, q, r, s(1, 3, 4, 5, 6, 7, 9, 12, 13, 14)$
(ii) $f(X) = \pi\, A, B, C, D\ (3, 5, 6, 7, 13) + d(1, 2, 4, 12, 15)$

OR

5 (a) What are different data types available in VHDL? Explain.

(b) Explain the structure of various LOOP statements in VHDL with examples.

UNIT - III

6 (a) Write VHDL code for 4-bit look ahead carry generator.

(b) Explain about three state devices.

OR

7 Explain about comparator and design a 16-bit comparator using 74x851C's. Write VHDL program.

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UNIT - IV

8 (a) Implement 32 input to 5 output priority encoder using four 74LS148 & gates.

(b) Draw the logic diagram of universal shift register and explain its operation.

OR

9 (a) Write a VHDL program for fixed point to floating point conversion.

(b) Design a conversion circuit and Write a data-flow style VHDL program to convert a D flip-flop to J-K flip-flop..

UNIT - V

10 (a) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.

(b) With the help of timing waveforms, explain the read and write operations of static RAM.

OR

11 (a) Draw the block diagram of synchronous RAM and explain its operation.

(b) Write short notes on EPROM.

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