Code: 13A04509 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations June 2017

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define CMRR.
(b) What do you mean by input offset current and offset voltage?
(c) What is the difference between inverting and non-inverting amplifier.
(d) List the applications of PLL.
(e) Define the term noise margin.
(f) What is meant by comparator?
(g) What are the data types available in VHDL?
(h) Write syntax of entity block in VHDL.
(i) Define encoder and decoder.
(j) Differentiate between latch and flip-flop.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Explain the pole-zero compensation technique.
(b) Explain about 741 Op-amp features.

OR

3 (a) Explain the working of instrumentation amplifier.
(b) Draw the equivalent circuit of the practical op-amp and explain the voltage transfer curve of the op-amp.

UNIT – II

4 (a) Explain how frequency multiplication is done using PLL.
(b) Explain the working of voltage controlled oscillator.

OR

5 With the help of neat internal functional diagram, explain the working of IC 555 as a Astable Multivibrator.

UNIT – III

6 (a) Explain sinking current and sourcing current of TTL output. Which of the parameters decide the fan-out and how?
(b) Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs.

OR

7 (a) Explain TTL inverter operation with neat diagram and transfer characteristics.
(b) Design a TTL two input NAND gate and explain the operation with the help of function table.

UNIT – IV

8 (a) Discuss the steps in VHDL design flow.
(b) Explain the use of packages. Give the syntax and structure of a package in VHDL.

OR

9 Write a behavioral style VHDL program for Barrel shifter.

UNIT – V

10 (a) Design Binary to Gray code converter and explain its procedure in detail.
(b) Write about three state devices and Parity circuits.

OR

11 (a) Implement S-R flip flop using D-flip flop.
(b) Write VHDL program for priority encoder.

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