

Code: 9A04605

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2017

**VLSI DESIGN**

(Common to ECE, EIE &amp; E.Con.E)

Time: 3 hours

Max. Marks: 70

Answer any FIVE questions  
All questions carry equal marks

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- 1 (a) Explain high pressure oxidation method for IC fabrication.  
(b) Explain the fabrication process of n-well CMOS transistor with neat diagrams.
- 2 (a) Describe the different operating regions of MOS transistor.  
(b) Find the drain-to-source current versus voltage relationship of  $I_{ds}$  Vs  $V_{ds}$  of n-MOS transistor.
- 3 (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.  
(b) Discuss the scaling factors for the following device parameters:  
(i) Gate capacitance.  
(ii) Maximum operating frequency.  
(iii) Current density.  
(iv) Power dissipation per gate.
- 4 (a) Explain the scan-path design technique used to test sequential circuits in detail.  
(b) Explain briefly about wiring capacitances associated with the layers.
- 5 (a) Design a 32 bit parallel adder optimized for speed, single-cycle operation and regularity of layout.  
(b) Compare the advantages and disadvantages of NAND ROMs and NOR ROMs.
- 6 (a) Explain how pass transistors are used to connect wire segments for the purpose of FPGA programming.  
(b) Draw the UV erasable EPROM structure for the programming of PAL device and explain how it programmed.
- 7 (a) Write a VHDL program to build N-bit ripple carry adder from N full adders.  
(b) What are the different data types available in VHDL and how they are indicated?
- 8 (a) Explain how a logic level simulation can verify complex circuits compared to other simulations.  
(b) What is the difference between design capture tools and design verification tools? Give some examples of each.

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