Code: 9A05704

R09

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2017

ADVANCED COMPUTER ARCHITECTURE

(Computer Science & Systems Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Discuss briefly about the VLSI complexity model.
(b) Define data dependence. Explain different types of data dependencies.

2 Define speed up and how Amdahl's law can be used to find the speed up of a computer system

3 How close a read dynamically scheduled, speculative processor come to ideal processor? Explain.

4 (a) Explain about addressing modes of signal processing.
(b) Explain the communication between processes in multi process environment.

5 (a) Explain briefly about the CM-S network architecture.
(b) Explain the characteristics of CRAY.

6 (a) Explain about the distributed coherent caches.
(b) What are the context-switching palivies adopted by the different multithread?

7 (a) Discuss various limitations of ILP construction level parallelism.
(b) Explain Branch prediction.

8 Differentiate between implicit and explicit parallelism with a neat diagram.

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