Code: 9A10504 **R09**

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2017

LINEAR & DIGITAL I.C APPLICATIONS

(Common to EEE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks

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1 (a) Explain the term “Slew rate” and how it affects the frequency response of an OP-AMP.
(b) Define the terms: CMRR, PSRR, input bias current, input offset voltage and gain band width product.

2 (a) Design a practical integrator circuit to properly process input sinusoidal waveforms up to 1 kHz. The input amplitude is 10 mV.
(b) Design a differentiator that will differentiate an input signal with $f_{max} = 100\ Hz$.

3 (a) Discuss, with relevant circuits and waveforms, the working of monostable multivibrator using 555 timer.
(b) Draw the circuit of a PLL AM detector and explain its operation.

4 (a) Explain steady state electrical behavior of CMOS circuit.
(b) Draw neat circuit diagram, function table and logic symbol of a 2-input CMOS NAND gate.

5 (a) What are the advantages and disadvantages of ECL?
(b) Explain CMOS/TTL interfacing with relevant diagrams.

6 (a) Write the syntax of a VHDL function definition and write a VHDL function for converting STD_LOGIC_VECTOR to INTEGER.
(b) Explain the concept of simulation and synthesis in terms of VHDL hardware description language.

7 Draw the traditional logic symbol, truth table, logic diagram of a standard MSI 74x151 8-input, 1-bit multiplexer and model the same using data flow-style VHDL program.

8 (a) Design a 4-bit binary synchronous counter using SSI 74x 74 D flip-flops.
(b) Write VHDL program for the logic shown in (a) using data flow style.

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