

R13

Code No: 114AF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**B.Tech II Year II Semester Examinations, May - 2016****DIGITAL DESIGN USING VERILOG HDL****(Electronics and Communication Engineering)****Time: 3 Hours****Max. Marks: 75****Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART - A**(25 Marks)**

- 1.a) What is functional verification? [2]
- b) Write short notes on programming language Interface. [3]
- c) Define tri-gate state. [2]
- d) What is array of Instances of primitives? [3]
- e) Define Initial Construct. [2]
- f) Define Blocking and Non-Blocking assignments. [3]
- g) Explain Bi-Directional gates. [2]
- h) Explain parameter declaration and assignments. [3]
- i) Explain Feedback model. [2]
- j) Explain test bench techniques. [3]

PART - B**(50 Marks)**

2. Define the following terms relevant to Verilog HDL.
 - a) Simulation versus synthesis
 - b) PLI
 - c) System Tasks. [3+3+4]

OR

- 3.a) Explain port declaration with an example using Verilog code.
- b) Write about white space characters and variables with examples. [5+5]
- 4.a) What is a three-state gate and explain each type of three-state gate with truth tables?
- b) Design module and a test bench for a half-adder. [5+5]

OR

- 5.a) Explain NMOS enhancement with conditions.
- b) Write a Verilog HDL code for n-bit right-to-left shift register using data flow level. [5+5]

- 6.a) What is difference between an Intra statement delay and an Inter statement delay? Explain using an example.
- b) Write the differences between begin-end and fork-blocks with examples. [5+5]

OR

- 7.a) Write syntax for while loop and write a Verilog code for n-bit Johnson counter.
- b) What is the difference between a sequential block and a parallel block? Explain using an example. [5+5]

8.a) Design half-adder using CMOS switches.

b) Write about basic switch primitives. [5+5]

OR

9.a) What do you mean by user defined primitives (UDP) and explain the types with examples?

b) Explain edge sensitive path using an example. [5+5]

10.a) What are the rules to be followed to declare and use the bidirectional lines?

b) Write a Verilog module for PLA. [5+5]

OR

11.a) Explain in detail about formal verification of a system.

b) What is the use of assert cycle sequence and assert next? Explain using an example. [5+5]

--ooOoo--