R13

Code No: 114DT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, May - 2016

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **(25 Marks)**

1.a)	What is Gray code?	[2]
b)	How do you obtain dual of an expression?	[3]
c)	What are don't cares?	[2]
d)	What is minterm?	[3]
e)	Compare combinational and sequential circuits.	[2]
f)	Explain about binary cell.	[3]
g)	What are the basic types of shift registers?	[2]
h)	Compare asynchronous and synchronous counters.	[3]
i)	Explain capabilities of finite state machine.	[2]
j)	Explain concept of minimal cover table.	[3]

PART – B **(50 Marks)**

2.a) Convert the given Gray code number to equivalent binary 0010010111110010.
b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal. [5+5]

OR

3.a) Obtain dual of the following Boolean expressions
i) AB+A(B+C)+B′(B+D).
ii) A+B+A′B′C.
b) Obtain the compliment of the following Boolean expressions
i) A′B+A′BC′+A′BCD+A′BC′D′E
ii) ABEF+ABE′F′+A′B′EF. [5+5]

4.a) Minimize the following expression using K-map and realize using NAND Gates.
F (A,B,C,D) = ∑m (0,1,2,9,11) +d(8,10,14,15).
b) Minimize the following expression using K-map and realize using NOR Gates.
f = π M(0,4,6,7,8,12,13,14,15). [5+5]

OR

5.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
b) Realize the function f(A,B,C,D)=π(1,4,6,10,14)+d(0,8,11,15) using:
i) 16:1 MUX
ii) 8:1 MUX. [5+5]

6.a) What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.

b) Draw and explain the circuit diagram of positive edge triggered J-K flip-flop using NOR gates with its truth table. How race around conditions are eliminated? [5+5]

OR

7. Explain in detail about timing and triggering considerations sequential circuits. [10]

8.a) Discuss about synchronous and ripple counters. Compare their merits and demerits.

b) What do you mean by universal shift register? Draw and explain its circuit diagram and operation. [5+5]

OR

9.a) What is a shift register? Explain about the following modes of operations in a four bit shift register (i) shift right (ii) shift left (iii) bidirectional.

b) Explain the differences between ring and Johnson counters. Design and explain the operation of a decade Johnson counters. [5+5]

10.a) What are the Moore and Melay machines? Compare them.

b) Explain the procedure for state minimization using the partition technique. [5+5]

OR

11.a) Name the elements of an ASM chart and define each one of them.

b) Explain the control subsystem implementation of weighing machine. [5+5]

--ooOoo--